Specification Amendments:

Please amend the following paragraphs as identified from the published application (2005/0228646) and the originally filed specification as follows.

Page 5, lines 21-29 of the originally filed specification or paragraph 0021 in the published application No. 2005/0228646:

[0021] The broadcast router components 102, 104, 106 and 108 will now be described in greater detail. FIG. 2 shows the first broadcast router component 102. The second, third and fourth broadcast router components 104, 106 and 108, on the other hand, are similarly configured to the first broadcast router component 102 and need not be described in greater detail. Of course, it should be clearly understood that certain components of the foregoing description of the first broadcast router component 102, as well as the second, third and fourth broadcast routers 104, 106 and 108 have been simplified for brevity of description. It is noted, however, that further details thereof may be found by reference to co-pending U.S. patent application Ser. No. 10/_____ 10/518,212 (Atty. Docket No. IU020160) and previously incorporated by reference.

Page 10, line 23 – page 11, line 10 of the originally filed specification, or paragraph 0031 in the published application No. 2005/0228646:

[0031] As may be seen in FIG. 4, the AES bi-phase decoder 296-1 is comprised of a time extraction circuit 297, a decoding logic circuit 298, a bit time estimator 300 and an appropriately sized data store, for example, a 32-bit wide asynchronous first-in-first-out ("FIFO") memory 302. The AES bi-phase decoder 296-1 receives the serialized digital audio data stream of AES data from the AES input 140-1. Within the AES bi-phase decoder 296-1, the AES serialized digital audio data stream is then routed to each of the time extraction circuit 297, the decoding logic circuit 298 and the bit time estimator 300. The time extraction circuit 297 extracts certain time information, specifically, the number of fast clocks separating successive preambles from the second serialized digital audio data stream. The time extraction circuit 297 then passes the extracted time information to the decoding logic circuit 298 for

decoding of the AES serialized digital audio data stream. Further details regarding the operation of the time extraction circuit 297 are set forth in greater detail in co-pending U.S. patent application Ser. No. 10/_____ 10/518,569 (Atty. Docket No. IU020254) and previously incorporated by reference. In addition to passing the extracted time information to the decoding logic circuit 298, the time extraction circuit 297 also passes the extracted time information to a selector circuit (not shown), having a control input tied to the control input for the selector circuit 138-1, which selects either the time information extracted from the AES serialized digital audio data stream on input 140-1 or the time information extracted from the AES serialized digital audio data stream on input 142-1 for forwarding to the routing engines 144 and 152.

Page 14, line 23 – Page 14, line 29 of the originally filed specification, or paragraph 0044 of the published application No. 2005/0228646:
[0044] It is possible to both identify preambles in the incoming serialized digital audio data stream and identify the type of preamble arriving because of the particular manner in which the preamble is encoded. As more fully described in co-pending ~~U.S. patent~~ PCT application ~~Ser. No. 10/_____~~ PCT/US03/19392, WO 2004/002060 (Atty. Docket No. IU020157), while the preamble for each subframe of the input digital audio data streams 1 through 4N is 4-bits long and has, therefore, a duration of 4 bit times, the preambles are encoded as a series of four pulses of irregular duration which, length as described in Table I, below.